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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,250	11/20/2001	Robertus Mominicus Joseph Verhaar	NL 000627	9630

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,250	VERHAAR ET AL.	
	Examiner	Art Unit	
	Chuong A Luu	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

REJECTION NOT BASED UPON PRIOR ART

Statutory Basis

Claim Rejections - 35 USC § 112

Claim 1 recites the limitation "the silicon surface" in line 5. There is insufficient antecedent basis for this limitation in the claim.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1-2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen et al. (U.S. 5,665,620) in view of Wang et al. (U.S. 4,376,672).

Nguyen discloses a method for forming concurrent top oxides using reoxidized silicon in an EPROM with

(1) a substrate (12) having a patterned ONO insulating layer (22, 24, 30) (see Figure 6) over a portion thereof, and characterized by the steps of forming an insulating layer comprising an Oxide-Nitride-Silicon layered structure (16, 18, 20) on the substrate (12) (see column 2, lines 66-67 and column 3, lines 1-37. Figures 2-4),

subsequently re-oxidizing the silicon layer (see column 2, lines 55-57) of the remaining Oxide-Nitride-Silicon structure (16, 18, 20) so as to form an ONO insulating layer structure (22, 24, 30) (see Figure 6);

(2) wherein the silicon layer (20) comprises an amorphous silicon layer (see column 3, lines 15-16);

(6) wherein the silicon layer is re-oxidized into a thermal oxide (see column 3, lines 56-59).

Nguyen teaches the above outlined features except for applying a photoresist to the silicon surface as part of a patterning process and stripping the photoresist once a required patterning process has been completed. However, Wang discloses a method for etching a layer of oxides with **(1).....** applying a photoresist (20) to the insulating material (15) (silicon surface) as part of a patterning process (see column 3, lines 20-29; column 7, lines 20-28) and stripping the photoresist (20) once a required patterning process has been completed (see Figure 3). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to combine the teachings of Nguyen and Wang (in accordance with the teaching of Wang) to apply a photoresist

to a silicon layer during etching process to protect it (the silicon layer) from damage while fabrication of a semiconductor device.

Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen et al. (U.S. 5,665,620) in view of Wang et al. (U.S. 4,376,672) and further in view of Shin et al. (U.S. 6,180,457 B1).

Nguyen and Wang teach everything above except for wherein a non-volatile memory cell is applied as part of the semiconductor structure, which non-volatile memory cell employs the ONO insulating layer between a floating gate and control gate thereof; wherein a non-volatile memory cell is applied with a control gate formed from a conductive layer which also serves to form part of a peripheral semiconductor structure; wherein the subsequent oxidation of the silicon sub-layer of the Oxide-Nitride-Silicon insulating layer takes place also to provide a high voltage oxide layer for a peripheral structure. Furthermore, Shin discloses a method of fabricating non-volatile semiconductor device with **(3)** wherein a non-volatile memory cell is applied as part of the semiconductor structure, which non-volatile memory cell employs the ONO insulating layer between a floating gate and control gate thereof (see column 6, lines 47-67. Figure 13); **(4)** wherein a non-volatile memory cell is applied with a control gate formed from a conductive layer which also serves to form part of a peripheral semiconductor structure (see column 7, lines 11-42; column 11, lines 58-65 and column 12, lines 9-10); **(5)** wherein the subsequent oxidation of the silicon sub-layer of the Oxide-Nitride-Silicon, which becomes Oxide-Nitride-Oxide or ONO, insulating layer

takes place also to provide a high voltage oxide layer for a peripheral structure (see column 6, lines 52-64). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to combine the above teachings of Nguyen, Wang and Shin to fabricate a non-volatile memory structure (in accordance with the teaching of Shin) with ONO is positioned between control gate and floating gate and a control gate formed from a conductive layer which also serves to form part of a peripheral semiconductor structure. Even though, Shin is silent about the ONO layer as a high voltage oxide, it is inherently that one having ordinary skill in the art would recognize that structure with same material would perform its function same as claimed. Doing so would increase the retention time of a non-volatile device.

Response to Arguments

Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that Lin fails to recite or suggest all the claimed limitations of Applicants' claim 1 on page 5. However, Nguyen discloses a method for forming concurrent top oxides using reoxidized silicon in an EPROM (see column 2, lines 55-67 and column 3, lines 1-37. Figures 2-4, 6). Also, Wang discloses a method for etching a layer of oxides (see column 3, lines 20-29; column 7, lines 20-28. Figure 3). Furthermore, Shin discloses a method of fabricating non-volatile semiconductor device (see column 6, lines 47-67; column 7, lines 11-42; column 11, lines 58-65 and column 12, lines 9-10. Figure 13). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to combine the above teachings of to

fabricate a non-volatile memory structure (in accordance with the teachings of Wang) to apply a photoresist to a silicon layer during etching process to protect it (the silicon layer) from damage while fabrication of a semiconductor device and (in accordance with the teachings of Shin) with ONO is positioned between control gate and floating gate and a control gate formed from a conductive layer which also serves to form part of a peripheral semiconductor structure and wherein the subsequent oxidation of the silicon sub-layer of the Oxide-Nitride-Silicon, which becomes Oxide-Nitride-Oxide or ONO, insulating layer takes place also to provide a high voltage oxide layer for a peripheral structure to increase the retention time of a non-volatile device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (703)305-0129. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Chuong Anh Luu
Patent Examiner